Institute of Computer Technology

B. Tech Computer Science and Engineering

Subject: Computer Organization (2CSE205)

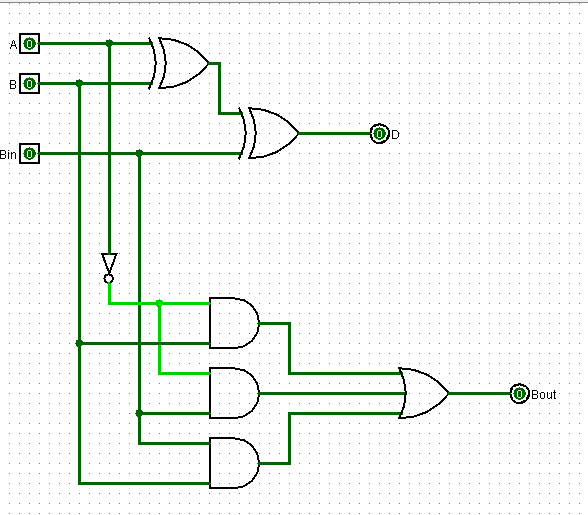
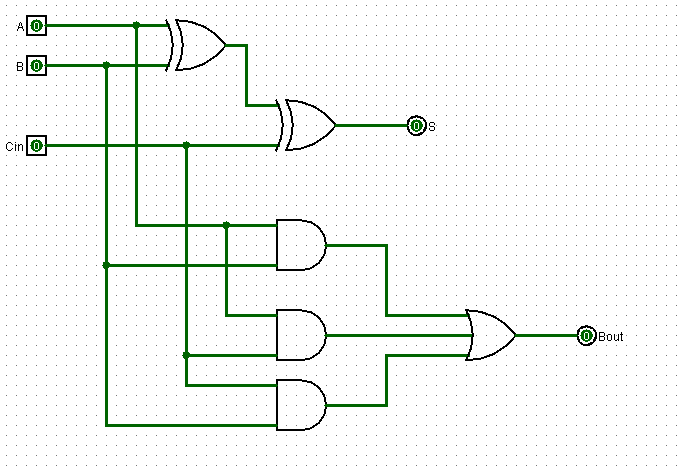
**PRACTICAL-1**

**AIM: - Introduction of Tool Logisim and revision on basic Logic gates**

**Exercise: -**

**1. Build Logical Circuit for Full Adder/ Subtractor using Logisim tool.**

**ANS:**

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**2. What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given below?**

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**ANS:**

={[(P+Q)’+(Q+R)’]’+[(P+R)’+(Q+R)’]’}’

=[(P+Q)’+(Q+R)’]’’[(P+R)’+(Q+R)’]’’

=[(P+Q)’+(Q+R)’][(P+R)’+(Q+R)’]

=(P’Q’+Q’R’)(P’R’+Q’R’)

=[Q’(P’+R’)][R’(P’+Q’)]

=Q’R’(P’+R’)(P’+Q’)

=Q’R’(P’+Q’R’)

=(P’Q’R’+Q’R’\*Q’R’)

=P’Q’R’+Q’R’

=Q’R’(P’+1)

=Q’R’\*1 =Q’R’

**3. Given f1, f3 and f in canonical sum of products form (in decimal) for the circuit given circuit:**

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**ANS:**

f1 \* f2 + f3 = f

Σm(4,5,6,7,8) \* f2 + Σm(1,6,15) = Σm(1,6,8,15)

By logically solving or by using the set theory method we can get the answer which is **option(c) Σm(6,8)**

**4. Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?**

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***SOLUTION***

Input for 1st flip flop is R=0 so (P+1) =0

Input for 2nd flip flop is (R+P)’= 1 so (Q+1) =1

Input for 3rd flip flop is (Q+R’) =1 so (R+1) =1

Therefore, Answer is 0, 1, 1 for P, Q, R respectively.

**5. In the sequential circuit shown below, if the initial value of the output Q1Q0 is 00, what are the next four values of Q1Q0?**

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***SOLUTION***

For first flip flop if T=1 and Q0=0 then (Q0+1) =1 and so on

For second flip flop if T=1 and Q1=0 then (Q1+1) =1 and so on

Next for values will be 1, 0, 1, 0 for both Q0, Q1.